REMARKS/ARGUMENTS

In the Office Action mailed September 4, 2008, claims 1-18 were rejected. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are canceled.

For reference, claims 1 and 8 are amended. In particular, claim 1 is amended to recite a plurality of distinct physical banks which facilitate serving read/write requests independently of each other to allow concurrent transfers for at least two of the physical banks. Claim 8 is amended to recite similar limitations. These amendments are supported, for example, by the subject matter described at page 5, lines 12-20, of the present application.

Additionally, claims 19 and 20 are added. Claim 19 recites each physical bank of memory modules is located on a separate DRAM module. Claim 20 recites similar limitations. These claims are supported, for example, by the subject matter described at page 5, lines 3-20, of the specification, as well as the correlation between the illustrations of Figs. 1 and 2 of the present application.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 4, 5, and 7-11 were rejected under 35 U.S.C. 102(b) as being anticipated by Emma et al. (U.S. Pat. No. 5,584,002, hereinafter Emma). Additionally, claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Asher (U.S. Pat. No. 6,671,822, hereinafter Asher). Additionally, claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer). Additionally, claims 11, 13, 17, and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Arimilli et al. (U.S. Pat. No. 5,978,888, hereinafter Arimilli). Additionally, claims 12 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Leung et al. (U.S. Pat. No. 5,829,026, hereinafter Leung). However, Applicants respectfully submit that these claims are patentable over Emma, Asher, Kramer, Arimilli, and Leung for the reasons provided below.

As a preliminary matter, it should be noted that claim 11 is rejected under both 102(b) and 103(a). However, the rejection of claim 11 under 102(b) based on Emma appears to be an error because the Office Action acknowledges, within the rejection of claim 11 under 103(a), that Emma does not teach all of the limitations of the claim. Applicant respectfully requests clarification as to the correct status of the rejections of claim 11.

Independent Claim 1

Claim 1 recites "remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules" (emphasis added). For a proper understanding of the first and second physical banks, claim 1 also recites "wherein each physical bank comprises some of the memory modules and is configured to facilitate serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks" (emphasis added). Thus, although the physical banks together make up the cache memory, each physical bank is nevertheless a separate physical device which can concurrently, but separately, process read/write requests independently from the other physical banks.

In contrast to the indicated limitation of claim 1, Emma does not disclose remapping memory modules from one physical bank to another physical bank which is physically and functionally separate from the other physical banks. More specifically, Emma does not disclose remapping memory modules from one physical bank to another physical bank within a cache memory which includes distinct physical banks that facilitate serving read/write requests independently of one another to allow concurrent transfers, as recited in the claim.

Emma merely addresses the historic cache synonym problem in which address references within a cache synonym class ambiguously reference addresses which have the same non-translatable address field but different translatable address bits. Emma, col. 2, line 63, through col. 3, line 9. More specifically, Emma describes a cache system to remap data in response to a hardware failure that disables a congruence class. Emma,

col. 3, lines 54-59. A congruence class simply identifies a limited group of locations in the cache at which data from a given memory address may be stored. Emma, col. 1, lines 39-42. In particular, each row within the cache forms a congruence class. Emma, col. 1, lines 61-63. Emma further explains that the loss of a single storage element in a set associative cache only disables one set of the congruence class. Emma, col. 2, lines 46-48. Additionally, Emma explains that it is possible to increase the number of congruence classes without changing set associativity. Emma, col. 2, lines 53-56. This description illustrates that the congruence classes are merely logical designations, rather than physical components within the cache. Hence, the congruence classes of Emma are not first and second physical banks, as recited in the claim, because the congruence classes are merely logical designations and are not physical banks of memory modules within the cache.

The present Office Action contends that the physical addresses corresponding to a given congruence class constitute a bank. While the interpretation asserted in the Office Action is not supported by any disclosure of the cited reference, the Office Action's characterization of Emma is nevertheless moot in view of the present amendments because Emma does not disclose a cache memory which includes distinct physical banks that facilitate serving read/write requests independently of one another to allow concurrent transfers. Emma merely describes a relatively small number of high-speed "data storage elements" which are used in the cache. Emma, col. 1, lines 16-21. However, Emma does not appear to describe any relationship between the logical designation of the congruence classes and the physical addresses of the data storage elements within the cache. In particular, Emma does not describe congruence classes which might correspond with particular data storage elements within the cache. Moreover, Emma does not describe any functionality to allow concurrent transfers on separate data storage elements. In other words, Emma does not describe any functionality to facilitate serving a read or write request on one of the data storage devices independently of the other data storage devices. Therefore, although Emma mentions the possibility of using a small number of data storage devices within the cache, Emma fails to describe serving a read/write request on one data storage element

independently of the other data storage elements to allow concurrent transfers for at least two of the data storage elements.

Therefore, Emma does not disclose all of the limitations of the claim because the logical congruence classes in Emma are not physical banks of memory modules. Furthermore, the physical addresses in a given congruence class do not constitute a physical bank, within the scope of the claim. Thus, Emma does not disclose remapping memory modules from one physical bank to another physical bank within a cache memory which includes distinct physical banks that facilitate serving read/write requests independently of one another to allow concurrent transfers, as recited in the claim. Accordingly, Applicants respectfully submit claim 1 is patentable over Emma because Emma does not disclose all of the limitations of the claim.

<u>Independent Claim 8</u>

Applicants respectfully assert independent claim 8 is patentable over Emma at least for similar reasons to those stated above in regard to the rejections of independent claim 1. In particular, claim 8 recites "performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits <u>remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules</u>" (emphasis added). Claim 8 also recites "the memory modules are distributed among a plurality of distinct physical banks within the cache memory, and each physical bank is configured to facilitate <u>serving a read/write request independently of the other physical banks</u> to allow <u>concurrent transfers</u> for at least two of the physical banks" (emphasis added).

Here, although the language of claim 8 differs from the language of claim 1, and the scope of claim 8 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejections of claim 1 also apply to the rejections of claim 8. Accordingly, Applicants respectfully assert claim 8 is patentable over Emma because Emma does not disclose remapping memory modules between physical banks of memory modules within a cache memory which includes distinct physical banks that facilitate serving read/write requests independently of one another to allow concurrent transfers, as recited in the claim.

Dependent Claims

Claims 2-7 and 9-20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8. Applicants respectfully assert claims 2-7 and 9-20 are allowable based on allowable base claims. Additionally, each of claims 2-7 and 9-20 may be allowable for further reasons, as discussed below.

In regard to the rejections of claims 11, 13, 17, and 18, Applicants submit that the claims are patentable over the combination of Emma and Arimilli because the Office Action does not show how the combination of cited references teaches all of the limitations of the claims. Claim 11 recites "the remapping means is further configured to remap at least one of the memory modules from an index within the first physical bank of memory modules to a new way and a different index within the second physical bank of memory modules." Claim 13 recites "the remapping means is further configured to remap at least one of the memory modules to a new way and a same index within the second physical bank of memory modules." Claims 17 and 18 recite similar limitations. However, the Office Action does not show how these limitations might be taught by the combination of cited references because the Office Action merely addresses the possibility of certain functionality. Although Arimilli may teach an arbitrary assignment of particular address to particular a congruency class, as asserted in the Office Action, the mere teaching of such arbitrary assignment <u>does not teach the actual limitations of the claims</u>. Furthermore, the mere possibility that the arbitrary assignment of Arimilli might <u>allow</u> certain functionality is not sufficient to show that Arimilli actually <u>teaches</u> the indicated functionality. In other words, the possibility of remapping a memory module in a certain way is <u>not taught</u> simply because such remapping might be <u>possible</u>. Furthermore, the Office Action does not assert that it would have been obvious to implement the functionality described in the present application in light of the actual teachings of Arimilli and Emma. Rather, the Office Action merely asserts that it would have been obvious to combine the teachings of Arimilli and Emma. However, since Arimilli does not teach the recited functionality, the assertion to combine the actual teachings of Arimilli and Emma nevertheless fails to teach all of the limitations of the claims. Therefore, since the mere <u>possibility</u> of implementing certain functionality is not part of the <u>actual teachings</u> of Arimilli and Emma, the proposed combination of Arimilli

and Emma fails to teach the indicated limitations of the claims. Accordingly, Applicant respectfully requests that the rejections of claims 11, 13, 17, and 18 be withdrawn.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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